AMENDMENTS TO THE SPECIFICATION

Please the following amendments to the specification:

Paragraph bridging Pages 2 and 3:

A solution is proposed in Proceedings of EOS/ESD Symposium, 1992, pages 277 to 288. Figure 2 illustrates the prior art vertical diode disclosed in the Proceedings. Reference numeral 70 designates a p-type silicon substrate. Two n-type wells 71 and 72 are formed in the p-type silicon substrate 70, and ~~ad~~ are spaced from one another. Shallow trench isolations 73 are employed in the prior art vertical diode. A single n-type impurity region 74 and two n-type impurity regions 74 are formed in a surface portion of the n-type well 71 and a surface portion of the other n-type well 72, respectively, and a p-type impurity region 75 is formed in a surface portion of the n-type well 72 between the n-type impurity regions 74 in the n-type well 72. A p-type impurity region 75 is further formed in a surface portion of the p-type silicon substrate 70 between the n-type well 71 and the other n-type well 72. The shallow trench isolations 73 are provided between the p-type silicon substrate 70, the n-type impurity region 74, the p-type impurity region 75, the n-type impurity region 74, the p-type impurity region 75, the n-type impurity region 74 and the p-type silicon substrate 70.

Paragraph bridging Pages 10 and 11:

Heavily-doped n-type source/ drain regions 17a/ 17b are formed in the p-type well 12, and are spaced from each other. Lightly-doped n-type source/ drain regions 18a/ 18b are formed inside of the heavily-doped n-type source/ drain regions 17a/ 17b, respectively, and are contiguous to the heavily-doped n-type source/ drain regions 17a/ 17b. A surface portion of the p-type well 12 serves as a channel region, and the channel region spaces the lightly-doped n-type drain region 18a ~~17a~~ from the lightly-doped n-type source region 17a ~~17b~~. The channel region and the lightly-doped n-type source/ drain regions 18a/ 18b are covered with a gate insulating layer 19, and a gate electrode 8 is formed on the gate insulating layer 19. The inner ends of the lightly-doped n-type source/ drain regions 18a/ 18b are self-aligned with both side surfaces of the gate electrode 8, respectively. Side wall spacers 9 are formed on both sides of the gate electrode 8, and the inner ends of the heavily-doped n-type source/ drain regions 17a/ 17b are self-aligned with the outer ends of the side wall spacers 9, respectively. The output terminal 1 is connected to the heavily-doped n-type drain region 17a, and the heavily-doped n-type source region l7b and the heavily-doped n-type impurity region 15 are connected to the ground line GND.

AMENDMENTS TO THE DRAWINGS

Applicant filed a clean set of Formal Drawings on November 30, 2001, and again on July 2, 2002. The PTO-948 form indicates that the drawings examined by the Official Draftsperson were filed on October 20, 1999. Applicant is again submitting Formal Drawings, and Applicant believes that the new Formal Drawings overcome the objection of the Official Draftsperson.

Attachment: Eleven (11) Replacement Sheets